Patent claims:

1. A nonvolatile memory cell

- having a vertical field-effect transistor with a nanoelement designed as the channel region;
- having an electrically insulating layer, which at least partially surrounds the nanoelement, as charge storage layer and as gate-insulating layer, which is designed in such a manner that
  - electrical charge carriers can be selectively introduced into or removed from it;
  - the electrical conductivity of the nanoelement can be influenced in a characteristic way by electrical charge carriers introduced in the electrically insulating layer.

2. The memory cell as claimed in claim 1, in which the electrically insulating layer is

- a silicon oxide/silicon nitride/silicon oxide layer sequence; or
- an aluminum oxide layer.

3. The memory cell as claimed in claim 1 or 2, in which the nanoelement includes

- a nanotube
- a bundle of nanotubes, or
- a nanorod.

4. The memory cell as claimed in claim 3, in which the nanorod includes

- silicon
- germanium
- indium phosphide
- gallium nitride
- gallium arsenide
- zirconium oxide and/or
- a metal.

5. The memory cell as claimed in claim 3, in which the nanotube is

- a carbon nanotube
- a carbon-boron nanotube
- a carbon-nitrogen nanotube
- a tungsten sulfide nanotube or
- a chalcogenide nanotube.

6. The memory cell as claimed in one of claims 1 to 5, which includes a first electrically conductive layer as first source/drain region of the field-effect transistor, on which the nanoelement is grown.

7. The memory cell as claimed in claim 6, in which the first electrically conductive layer is made from catalyst material for catalyzing the formation of the nanoelement.

8. The memory cell as claimed in one of claims 1 to 7, which includes a second electrically conductive layer as gate region of the field-effect transistor, which at least partially surrounds the electrically insulating layer.

9. The memory cell as claimed in claim 8, in which the thickness of the second electrically conductive layer is less than a longitudinal extent of the nanoelement, such that the electrically insulating layer which surrounds the nanoelement and the second electrically conductive layer form a ring structure surrounding part of the nanoelement.

10. The memory cell as claimed in one of claims 1 to 9, which includes a third electrically conductive layer as second source/drain region of the field-effect transistor, which third electrically conductive layer is formed on the nanoelement.

11. The memory cell as claimed in one of claims 1 to 10, formed on and/or in a substrate made from polycrystalline or amorphous material.

12. The memory cell as claimed in one of claims 1 to 11, which is formed exclusively from dielectric material, metallic material and the material of the nanostructure.

13. A memory cell array having a plurality of memory cells as claimed in one of claims 1 to 12 formed next to and/or on top of one another.

14. A method for fabricating a nonvolatile memory cell, in which

- a vertical field-effect transistor is formed with a nanoelement designed as the channel region;
- an electrically insulating layer, which at least partially surrounds the nanoelement, is formed as charge storage layer and as gate-insulating layer;
- the electrically insulating layer is designed in such a manner that
    - electrical charge carriers can be selectively introduced into or removed from it;
    - the electrical conductivity of the nanoelement can be influenced in a characteristic way by electrical charge carriers introduced in the electrically insulating layer.

15. The method as claimed in claim 14, in which

- a first electrically conductive layer is formed as first source/drain region of the field-effect transistor;
- then a second electrically conductive layer is formed as gate region of the field-effect transistor;

- a subregion of the first electrically conductive layer is uncovered by a via hole being introduced into the second electrically conductive layer;
- the electrically insulating layer is formed on the surface of the via hole;
- the nanoelement is grown in the via hole on the uncovered subregion of the first electrically conductive layer.

16. The method as claimed in claim 14, in which
- a first electrically conductive layer is formed as first source/drain region of the field-effect transistor;
- then an auxiliary layer is formed;
- a subregion of the first electrically conductive layer is uncovered by a via hole being introduced into the auxiliary layer;
- the nanoelement is grown in the via hole on the uncovered subregion of the first electrically conductive layer;
- the auxiliary layer is removed;
- the electrically insulating layer is applied to the surface of the nanoelement.

17. The method as claimed in claim 14, in which the nanoelement is initially grown vertically while standing freely on a source/drain region, and then the remainder of the vertical field-effect transistor is formed.